CLAIMS

What is claimed is:

1. A memory cell, comprising:

a semiconductor substrate having at least one trench formed in a surface thereof;

a recessed channel region of a first conductivity type semiconductor formed in the semiconductor substrate below each trench;

a source region and a drain region both of a second conductivity type semiconductor formed in the semiconductor substrate on opposing sides of each trench, wherein a bottom of the source region and a bottom of the drain region are above a floor of the trench;

a gate dielectric layer formed on the semiconductor substrate, said gate dielectric layer being formed along the bottom and sidewalls of the trench; and

a control gate formed over the gate dielectric layer above the recessed channel region.

2. The memory cell of claim 1, wherein the bottom of the source region and the bottom of the drain region are about 700 Angstroms to 1000 Angstroms above the floor of the trench.

3. The memory cell of claim 1, wherein the bottom of the source region and the bottom of the drain region are at a depth from a surface of the semiconductor substrate of about 40 percent to 60 percent of the depth of the floor of the trench from the surface of the semiconductor substrate.

4. The memory cell of claim 1, wherein the at least one trench sidewall is formed at an angle greater than 90 degrees with respect to a trench floor.

5. The memory cell of claim 1, wherein the thickness of the gate dielectric layer between the top surface of the gate dielectric layer and the bottom surface of the gate dielectric layer is between 220 and 270 angstroms in thickness.

6. The memory cell of claim 1, wherein the semiconductor substrate is a silicon-on-insulator (SOI) semiconductor substrate.

7. The memory cell of claim 1, wherein the semiconductor substrate is a bulk silicon semiconductor substrate.

8. The memory cell of claim 1, wherein the memory cell is a silicon-oxide-nitride-oxide-silicon (SONOS) device.

9. The memory cell of claim 8, wherein the gate dielectric layer is an oxide-nitride-oxide (ONO) layer.

10. The memory cell of claim 9, wherein the ONO layer is formed in the at least one trench region so as to insulate the nitride layer from a floor region and a plurality of sidewall regions within the trench region.

11. The memory cell of claim 9, wherein a bottom oxide layer of the ONO layer has a thickness of about 60 Angstroms to 80 Angstroms.

12. The memory cell of claim 1, wherein the gate dielectric layer extends above the source region and the drain region.

13. The memory cell of claim 1, wherein the control gate resides in the at least one trench.

14. The memory cell of claim 1, wherein the gate dielectric layer is comprised of a high-K dielectric material.

15. The memory cell of claim 1, wherein the gate dielectric layer is comprised of a standard-K dielectric material.

16. The memory cell of claim 1, wherein the at least one trench has an aspect ratio of about 100:1.

17. The memory cell of claim 1, wherein an upper surface of the control gate is substantially at the same level as an upper surface of the gate dielectric layer.

18. A method of fabricating a memory cell, comprising the steps of:

forming at least one trench in a semiconductor substrate;

forming a recessed channel region of a first conductivity type semiconductor in the semiconductor substrate at the bottom of each trench;

forming a source region and a drain region both of a second conductivity type semiconductor in the semiconductor substrate on opposing sides of each trench, wherein a bottom of the source region and a bottom of the drain region are above a floor of the trench;

forming a gate dielectric layer on the semiconductor substrate, said gate dielectric layer being formed along the bottom and sidewalls of the trench; and

forming a control gate over the gate dielectric layer above the recessed channel region.

19. The method of claim 18, wherein the step of forming the source region and the drain region includes forming the bottom of the source region and the bottom of the drain region about 700 Angstroms to 1000 Angstroms above the floor of the trench.

20. The method of claim 18, wherein the step of forming the source region and the drain region includes forming the bottom of the source region and the bottom of the drain region at a depth from a surface of the semiconductor substrate of about 40 percent to 60 percent of the depth of the floor of the trench from the surface of the semiconductor substrate.

21. The method of claim 18, wherein the step of forming at least one trench includes forming at least one trench side wall at an angle greater than 90 degrees with respect to a trench floor.

22. The method of claim 21, wherein the step of forming at least one trench side wall at an angle greater than 90 degrees with respect to a trench floor includes performing a directional etch.

23. The method of claim 18, further comprising the step of:

forming the gate dielectric layer between the top surface of the gate dielectric layer and the bottom surface of the gate dielectric layer between 220 and 270 angstroms in thickness.

24. The method of claim 18, further comprising the step of:

using a silicon-on-insulator (SOI) semiconductor substrate as the semiconductor substrate.

25. The method of claim 18, further comprising the step of:

using a bulk silicon semiconductor substrate as the semiconductor substrate.

26. The method of claim 18, further comprising the step of:

using an oxide-nitride-oxide (ONO) layer to form the gate dielectric layer.

27. The method of claim 26, further comprising the step of:

forming the ONO layer in the trench region so as to insulate the nitride layer from a floor region and a plurality of sidewall regions within the trench region.

28. The method of claim 26, further comprising the step of:

forming a bottom oxide layer of the ONO layer to a thickness of about 60 Angstroms to 80 Angstroms.

29. The method of claim 18, further comprising the step of:

extending the gate dielectric layer above the source region and the drain region.

30. The method of claim 18, further comprising the step of:

forming the control gate in the at least one trench.

31. The method of claim 18, further comprising the step of:

using a standard-K dielectric material to form the gate dielectric layer.

32. The method of claim 18, further comprising the step of:

using a high-K dielectric material to form the gate dielectric layer.

33. The method of claim 18, further comprising the step of:

forming the at least one trench to have an aspect ration of about 100:1.

34. The method of claim 18, further comprising the step of:

forming an upper surface of the control gate substantially at the same level as an upper surface of the gate dielectric layer.

35. The method of claim 34, wherein the step of forming an upper surface of the control gate substantially at the same level as an upper surface of the gate dielectric layer includes using chemical-mechanical planarization.

36. The method of claim 18, wherein the step of forming at least one trench in a semiconductor substrate includes using a directional etchant.

37. The method of claim 36, wherein the step of using a directional etchant includes a reactive ion etch.

38. A method of erasing a memory cell, comprising the steps of:

applying a negative potential to a control gate; and

applying a positive potential to a drain, wherein the negative potential and the positive potential produce hot hole tunneling from the drain to a charge trapping layer through an insulation layer.